IN THE CLAIMS

Please amend the claims as follows:

1. (presently amended) A data processing system, comprising:

a system memory for storing legacy code;

a central processing unit (CPU) in communication with said system memory;

~~legacy code stored in said system memory, wherein said legacy code is not optimized for said CPU;~~

a code-optimizing coprocessor in communication with said system memory and said CPU, wherein ~~; and control logic within said code-optimizing coprocessor that causes~~ said code-optimizing coprocessor ~~to~~ generates a plurality of optimized code from said legacy code to be stored within said system memory while said CPU is executing said legacy code, ~~such that~~ wherein said plurality of optimized code is ~~tailored to~~ more optimized for execution within said CPU than said legacy code; and

means for switching an execution of said legacy code by said CPU to an execution of said plurality of optimized code, in response to an encounter of a switch point.

2. (presently amended) The data processing system of Claim 1, wherein said data processing system further includes a switch point table for storing said switch point and other switch points, wherein said switch points identify specific instructions within said legacy code at which execution can be switched from said legacy code to said plurality of optimized code without any change to an architectural state of said CPU ~~code-optimizing coprocessor causes said CPU to automatically utilize said at least some optimized code in lieu of at least some of said legacy code, after said code-optimizing coprocessor has generated at least some optimized code~~.

3. (presently amended) The data processing system of Claim 1, wherein said data processing system further comprises

a translation look-aside buffer (TLB); and

means for generating ~~a TLB update channel that links said TLB to said code optimizing coprocessor and that said code optimizing coprocessor utilizes to generate~~ a page-table entry (PTE) for said plurality of optimized code in said TLB ~~after said code optimizing coprocessor has generated at least some of said optimized code~~.

4. (presently amended) The data processing system of Claim 3, wherein said CPU further comprises a program counter, wherein said code-optimizing coprocessor alters said program counter to point to said PTE for said plurality of optimized code after ~~said code optimizing coprocessor has utilized said TLB update channel to generate a page table entry (PTE)~~ said PTE has been generated for said plurality of optimized code in said TLB, thereby causing said CPU to automatically utilize said ~~at least some~~ plurality of optimized code in lieu of ~~at least some of~~ said legacy code.

5. (presently amended) The data processing system of Claim 1, wherein said data processing system further comprises a level-one (L1) cache for storing a subset of said plurality of ~~, and said code optimizing coprocessor responds to generation of at least some optimized code by automatically transferring said at least some~~ optimized code ~~to said L1 cache~~.

Please cancel Claims 6-20.